CLAIMS

1. A semiconductor device characterized in comprising a word line, a first bit line pair, a memory cell provided at an intersection of said word line and said first bit line pair, a second bit line pair, a switch circuit for coupling said first bit line pair and said second bit line pair, a sense amplifier including a first circuit connected to said first bit line pair and a second circuit connected to said second bit line pair, a first precharge circuit for precharging said first bit line pair to a first precharge potential and a second precharge circuit for precharging said second bit line pair to a second precharge potential, wherein

said second circuit amplifies one of said first bit line pair and one of second bit line pair to a first potential and the other of said first bit line pair and the other of said second bit line pair to a second potential from a storage signal of said memory cell,

said first precharge potential is ranged between said first and second potentials, and

said second precharge potential is said second potential.

2. A semiconductor device according to claim 1, characterized in that

said switch circuit isolates, in the first period during

the read operation of said memory cell, said first bit line pair and said second bit line pair and said first circuit amplifies a signal of said memory cell read on said first bit line pair and then outputs the signal to said second circuit, said switch circuit connects, in the subsequent second period, said first bit line pair and said second bit line pair and said second circuit respectively writes said first potential to one of said first bit line pair and said second potential to the other of said first bit line pair.

3. A semiconductor device according to claim 2, characterized in that

said first circuit includes a first MOSFET having a gate connected to one of said first bit line pair and a second MOSFET having a gate connected to the other of said first bit line pair with a source thereof connected to the source of said first MOSFET, and

said second circuit includes a latch circuit.

4. A semiconductor device according to claim 3, characterized in that

said latch circuit includes a P-type third MOSFET and a P-type fourth MOSFET in which the sources are connected in common and the gates and drains are cross-connected and an N-type fifth MOSFET and an N-type sixth MOSFET in which the drains are respectively connected corresponding to the drains of said third and fourth MOSFETs and the gates and drains are

cross-connected and the drains of said first and second MOSFETs are respectively connected to the sources of said fifth and sixth MOSFETs.

5. A semiconductor device according to claim 4, characterized in that

said second potential is impressed to the sources of said first to fourth MOSFETs in the period where said sense amplifier is not activated, and

said first potential is supplied to the sources of said first and second MOSFETs when said sense amplifier is activated.

6. A semiconductor device according to claim 3, characterized in that

said latch circuit includes a P-type third and a P-type fourth MOSFETs in which the sources are respectively connected in common and the gates and drains are cross-connected and an N-type fifth MOSFET and an N-type sixth MOSFET in which the sources are connected in common, the drains are respectively connected corresponding to the drains oaf said third and fourth MOSFETs and the gates and drains are cross-connected, and

the drains of said first and second MOSFETs are respectively connected to the drains of said fifth and sixth MOSFETs.

7. A semiconductor device according to claim 6, characterized in that

the sources of said first and second MOSFETs are connected to a first control line,

the sources of said fifth and sixth MOSFETs are connected to a second control line,

said first circuit starts the amplifying operation in said first period when the predetermined potential is impressed to said first control line, and

said second circuit starts the amplifying operation when said first potential is impressed to said second control line after said first period.

8. A semiconductor device according to claim 7, characterized in that

said second potential is impressed to said first and second control lines in the period where said sense amplifier is not activated, and

said predetermined potential impressed to said first control line is lower than said first potential when said sense amplifier is activated.

9. A semiconductor device according to claim 1, characterized in that

said first circuit includes a first MOSFET having the gate connected to one of said first bit line pair and a second MOSFET having the gate connected to the other of said first bit line pair with the source thereof connected to the source of said first MOSFET,

said second circuit includes a P-type third and a P-type fourth MOSFETs in which the sources are respectively connected in common and the gates and drains are cross- connected and an N-type fifth MOSFET and an N-type sixth MOSFET in which the sources are respectively connected in common, the drains are connected corresponding to the drains of said third and fourth MOSFETs and the gates and drains are cross-connected,

the drains of said first and second MOSFETs are respectively connected to the drains of said fifth and sixth MOSFETs,

the sources of said first and second MOSFETs are connected to said first control line, and

the sources of said fifth and sixth MOSFETs are connected to said second control line.

10. A semiconductor device according to claim 1, characterized in that

said first circuit includes a first MOSFET having the gate connected to one of said first bit line pair and a second MOSFET having the gate connected to the other of said first bit line pair with the source thereof connected to the source of said first MOSFET,

said second circuit includes a latch circuit including a plurality of third MOSFETs,

said switch circuit includes a fourth MOSFET in which a source/drain route is connected between one of said first

bit line pair and one of said second bit line pair and a fifth MOSFET in which a source/drain route is connected between the other of said first bit line pair and the other of said second bit line pair, and

said fourth and fifth MOSFETs respectively have the gate insulation films which are thicker than the gate insulation films of said first to third MOSFETs.

11. A semiconductor device according to any one of claims 1 to 10, characterized in that

said memory cell includes one capacitor connected to the source/drain route of one MOSFET, and

said second potential is higher than said first potential.

12. A semiconductor device according to claim 11, characterized in that

said first precharge potential is a half of said first potential and said second potential, and

a voltage difference of said first potential and said second potential is ranged between 0.5 to 1.8V.

13. A semiconductor device characterized in comprising a word line, a first bit line pair, a memory cell provided at an intersection of said first word line and said first bit line pair, a second bit line pair, a capacitor pair including a first capacitor having a first electrode connected to one of said first bit line pair and a second electrode connected to one

of said second bit line and a second capacitor having a third electrode connected to the other of said first bit line pair and a fourth electrode connected to the other of said second bit line pair, a switch circuit including a first switch for connecting one of said first bit line pair and one of said second bit line pair and a second switch for connecting the other of said first bit line pair and the other of said second bit line pair, a sense amplifier connected to said second bit line pair, a first precharge circuit for precharging said first bit line pair to a first precharge potential and a second precharge circuit for precharging said second bit line pair to a second precharge potential.

14. A semiconductor device according to claim 13, characterized in that

said sense amplifier amplifies one of said first and second bit line pairs to a first potential and the other to a second potential from a storage signal of said memory cell and said first precharge potential is ranged between said first potential and said second potential, and

said second precharge potential is said second potential.

15. A semiconductor device according to claim 13, characterized in that

said switch circuit isolates, in the first period during the read operation of said memory cell, said first bit line

pair and said second bit line pair and also outputs a signal stored in said memory cell to said first bit line pair, said sense amplifier is activated, in the subsequent second period, under the condition that said switch circuit isolates said first bit line pair and said second bit line pair, and said switch circuit connects, in the subsequent third period, said first bit line pair and said second bit line pair and thereby said sense amplifier writes said first potential to one of said first bit line pair and said second potential to the other of said first bit line pair, respectively.

16. A semiconductor device according to any one of claims 13 to 15, characterized in that

said first and second capacitors are respectively the N-type MOSFETs, in which the gates are used as one electrode and the sources and drains are connected in common as the other electrode.

17. A semiconductor device according to any one of claims 13 to 15, characterized in that

said memory cell includes one capacitor connected to the source/drain route of one MOSFET,

said sense amplifier includes a P-type first MOSFET pair in which the sources are respectively connected in common and the gates and drains are cross-connected and an N-type second MOSFET pair in which the sources are connected in common, drains are respectively connected corresponding to the drains of said

first MOSFET pair and the gates and drains are cross-connected, and

said second potential is higher than said first potential.

18. A semiconductor device according to claim 17, characterized in that

said first and second capacitors are N-type MOSFETs having the gates used as one electrode and the sources and drains which are connected in common as the other electrode.

19. A semiconductor device according to claim 14 or 4, characterized in that

a voltage difference between said first potential and said second potential is ranged between 0.5V to 1.8V.

20. A semiconductor device characterized in comprising a word line, a first bit line pair consisting of a first bit line and a second bit line, a memory cell provided at an intersection of said word line and said first bit line pair, a second bit line pair consisting of a third bit line and a fourth bit line, a first switch circuit for connecting said first bit line and said third bit line, a second switch circuit for connecting said second bit line and said fourth bit line and a sense amplifier connected to said second bit line pair, wherein

said sense amplifier amplifies the information stored in said memory cell to a first potential on said third bit line and to a second potential on said fourth bit line,

said first and second switch circuits isolate, in the first period during the read operation of said memory cell, said first and second bit lines pairs, and

said sense amplifier writes, in the subsequent second period, said first potential to said first bit line under the condition that said first switch connects said first bit line and said third bit line and said second switch circuit isolates said second bit line and said fourth bit line.

21. A semiconductor device according to claim 20, characterized in that

said second switch circuit of said semiconductor device connects, in the subsequent third period following the second period during the read operation of said memory cell, said second bit line and said fourth bit line and said sense amplifier writes said second potential to said second bit line.

22. A semiconductor device according to claim 20 or 21, characterized in that

a logic gate to which said second bit line pair is inputted is further comprised, and

said logic gate detects, in said first period, that said sense amplifier has driven one of said second bit line pair to said first or second potential and then starts the second periods.

23. A semiconductor device comprising:

a plurality of first and second word lines;

a first bit line pair including a first bit line and a second bit line;

a second bit line pair including a third bit line and a fourth bit line;

a plurality of first DRAM memory cells provided at an intersection of said first word lines and said first bit line;

a plurality of second DRAM memory cells provided at an intersection of said second word lines and said second bit line;

a first MOSFET having a source and drain path coupled to said first bit line and said second bit line;

a second MOSFET having a source and drain path coupled to said second bit line and said third bit line;

a sense amplifier coupled to said third and fourth bit lines;

a first control line coupled to a gate of said first MOSFET; and

a second control line coupled to a gate of said second MOSFET,

wherein during a rewriting operation one of said first and second MOSFETs is in on-state and the other of said first and second MOSFETs is in off-state.

24. The semiconductor device according to claim 23,

wherein during said rewriting operation said first and second control lines are set on different levels and said sense amplifier is used for rewriting to one of said first and second DRAM memory cells which is coupled to a selected word line of said plurality of first and second word lines, and

wherein said levels of said first and second control lines depend on a selection of said plurality of first and second word lines.

25. The semiconductor device according to claim 24, further comprising:

a third bit line pair including a fifth bit line and a sixth bit line;

a third MOSFET having a source and drain path coupled to said third bit line and said fifth bit line; and

a fourth MOSFET having a source and drain path coupled to said fourth bit line and said sixth bit line,

wherein said first and second MOSFETs each have a thicker gate insulating layer than said third MOSFET.

26. The semiconductor device according to claim 25, wherein said third bit line pair is a global bit line pair for write operation.

27. The semiconductor device according to claim 26, further comprising:

a fourth bit line pair including a seventh bit line and an eighth bit line;

a fifth MOSFET having a source and drain path coupled to said third bit line and said seventh bit line; and

a sixth MOSFET having a source and drain path coupled to said fourth bit line and said eighth bit line,

wherein said fourth bit line pair is a global bit line pair for read operation.

28. The semiconductor device according to claim 27, wherein after a first time period said levels of said first and second control lines are set on a same level.